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Soft breakdown in the bistable MOS tunnel structures

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Abstract. The S-shape reverse-bias characteristics of MOS tunnel structure on n-Si (d < 3 nm, $N_{\rm d} \approx 10^{16}~{\rm cm}^{-3}$) and their post-soft-breakdown transformation are analyzed. Turn-on voltages and holding voltages are found theoretically and measured. The change of these parameters with oxide damage is suggested to reflect a complicated interplay between the injection efficiency, energy distribution of injected electrons and conductivity of an inversion layer.

Introduction

MOS tunnel structures with 1–3 nm oxide thickness are now being intensively studied worldwide as components of future sub-0.1 μ m-channel MOSFETs [1] and of several other interesting devices, e.g. tunnel emitter transistors [2]. A central point of these studies is the reliability limitation by a soft breakdown (SB) which is defined as an appearance of non-extending local breakdown spot [3]. Along with values of a transported charge-to-breakdown, commonly used as the measure of reliability [3], it is, of course, very important to obtain information about the transformations of structure characteristics in general. Special attention deserves the case of reverse bias, as corresponding to a conventional operational mode of most MOS tunnel devices.

1. Reverse current-voltage characteristics

The reversely biased MOS tunnel structures on n-Si were shown to exhibit bistable behavior [2, 4] (Fig. 1). That the nature of this effect is Auger ionization is known long ago [4], but neither the parameters of an S-shape segment, nor their change after the SB of the oxide have been studied in detail earlier. The purpose of this work is twofold: first, we aim to determine the parameters (turn-on voltage $V_{\rm sw}$, holding voltage $V_{\rm h}$ and current), and secondly to clarify how these are changed after the soft breakdown in the oxide. A basic equation for a MOS structure under inversion is the balance equation:

$$\int j_{h} dS + \int j_{diff} dS = J_{ext} + \int j_{e}(M-1) dS$$
 (1)

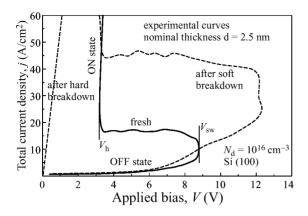
for minority carriers, where j_h and j_e are densities of hole and electron tunnel currents, $J_{\text{ext}} = (j_{\text{ext}}S)$ is eventual external hole supply, j_{diff} is density of hole diffusion current and M is carrier multiplication factor, S is for device area.

2. Model of electron energy relaxation

The process of hot electron thermalization in silicon can be divided into two stages (Fig. 2). The first one takes place just beyond the inversion layer and the second one proceeds in the space charge region (like in p-n-junction). Taking both these stages in mind, the multiplication factor can be written as:

$$M = (1+P)(1+\gamma) \tag{2}$$

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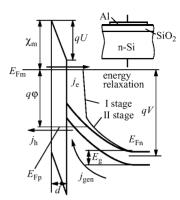


Fig. 1. Typical transformation of the reverse current-voltage characteristics (averaged current vs applied bias) of a MOS tunnel diode after the SB.

Fig. 2. Band diagram of an n-Si MOS tunnel structure under reverse bias.

$$P = \frac{1}{j_{\rm e}} \int_{0}^{+\infty} \frac{\mathrm{d}j_{\rm e}}{\mathrm{d}E} P_{\text{Auger}} \mathrm{d}E$$

$$\gamma = \frac{a_0 q N_{\rm d} w^2}{b_0 \varepsilon_0 \varepsilon_{\rm s}} \exp\left(-\frac{b_0 \varepsilon_0 \varepsilon_{\rm s}}{q N_{\rm d} w}\right), \quad a_0, b_0 = \text{const}$$
(3)

P denotes the effective quantum yield of Auger generation and γ of impact ionization (Fig. 3). In earlier studies, impact ionization was ignored. Integration over dE is to regard the energy distribution of injected electrons. The factor γ depends on the depletion layer width w (if $V \gg U$ it is a function of just V).

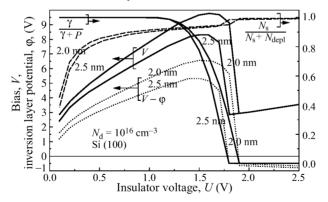


Fig. 3. Interrelation between the insulator voltage U, applied bias V and inversion layer potential φ . Relative contribution of impact/Auger ionization $\gamma/(\gamma+P)$, and of inversion layer/depletion layer charge $N_s/(N_s+N_{\rm depl})$.

3. OFF state

For an Al/SiO₂/n-Si structure, it is only the electron component that provides a total tunnel current in an OFF state (see Fig. 1 for notation) at moderate V. In our thickness range, the inversion layer does not exist in an OFF state. For this reason, the large-area device

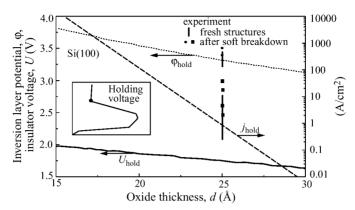


Fig. 4. Parameters of holding point of MOS tunnel structures for the case of low $N_{\rm d}$. Holding voltages $V_{\rm h}$ are by ~ 0.7 V lower than $\varphi_{\rm hold}$.

operates as a conjunction of multiple quasi independent MOS structures. Defect area, if any, turns to be isolated from the rest part of structure. As a result, only minor changes of the current–voltage curve after the SB can be seen (Fig. 1). This is in contrast to the accumulation case when the electrical conductivity along the Si/SiO₂ interface is large.

4. ON state

For a fresh and homogeneous structure, the parameters of the holding point (Fig. 4) may be found disregarding the contribution of depletion layer charge to the insulator voltage U. Further, in the ON state (Fig. 1), there is no impact ionization (P > 0, $\gamma = 0$). Therefore, we have for the voltage U at holding point:

$$P(E_{\text{eff}}) = \beta^{-1} \tag{4}$$

$$E_{\text{eff}} = qU + q\sqrt[3]{\frac{72}{11}} \left[\frac{\hbar \varepsilon_I}{\varepsilon_S \sqrt{qm_h}} \right]^{2/3} \left(\frac{U}{d} \right)^{2/3}$$
 (5)

where β is for the ratio of electron-to-hole tunneling currents. The second term in (5) regards the additional energy gain by monoenergetic [4] electrons while passing through inversion layer. In the ON state, higher from the holding point (Fig. 1), the insulator voltage and the diffusion current j_{diff} increase. The ON state of a MOS tunnel structure is very sensitive to the oxide degradation (Fig. 4). The matter is that the inversion layer tends to become equipotential along the whole structure, even if the oxide is locally destroyed. The leakage in one place strongly influences neighboring area. Oxide breakdown may cause the local changes of β and also the (local) changes in the transport mechanism which lead to the alterations of interrelation E(U).

5. Turn-on voltage

The value of a turn-on voltage (Fig. 5) is predominately determined by the impact ionization (see Fig. 3). In fact, the major contribution toward the insulator voltage is done by holes, while the extension of a depletion area was shown to play a minor role. Due to hole generation by impact ionization, the insulator voltage grows with increasing V in the OFF state. Except for the very weak inversion, injection efficiency β only insignificantly depends on U. Turn-on voltage is sensitive to the oxide degradation through the change of β

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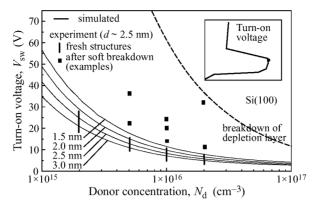


Fig. 5. Turn-on voltage of MOS tunnel structures. Its value after the oxide soft breakdown is limited by the breakdown of space charge area.

and P. In fact, calculations show that both P and γ give a substantial contribution toward the multiplication factor M (Fig. 3). With decreasing d, β decreases and $V_{\rm sw}$ therefore increases.

6. Conclusion

The transformations of reverse current–voltage characteristics of n-Si MOS tunnel structures resulting from a soft breakdown of the oxide layer have been considered. After the soft breakdown, both the turn-on voltage and the holding voltage have been shown to increase. Three factors are responsible for this: (a) decrease of MOS emitter injection efficiency with a reduction of the oxide thickness; (b) decrease of electron energy and quantum yield of Auger ionization inside the breakdown spot(s); (c) strong current crowding in the thinnest device sections.

Acknowledgements

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References

- [1] H. S. Momose et al., IEEE Trans. Electr. Dev. ED-45, 691 (1996).
- [2] I. V. Grekhov et al., Solid-State Electron. 38, 1533 (1995).
- [3] M. Depas et al., IEEE Trans. Electr. Dev. ED-43, 1449 (1996).
- [4] S. K. Lai et al., Appl. Phys. Lett. 38 41 (1981).